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(54) Title: STRUCTURED SILICON ANODE

(57) Abstract: A silicon/lithium battery which can be fabricated from a silicon substrate allowing it to be produced as an integrated unit on a chip, the battery comprising a silicon anode formed from sub-micron diameter pillars of silicon fabricated on an n-type silicon wafer.

Structured Silicon Anode

The present invention relates to structured silicon anodes for lithium battery applications.

Silicon is recognised as a potentially high energy per unit volume host material for lithium in lithium battery applications[1]. Attempts at realising this potential have met with only partial success when nano-composites of silicon powder and carbon black have been used[2]. The major technical problem associated with the use of silicon/lithium appears to be the mechanical failure brought about by the repeated large volume expansion associated with alloying[1c,3]. Metallic and intermetallic anodic host materials, other than layer materials such as graphite, are reported to disintegrate after a few lithium insertion/extraction cycles[3,4] unless in fine powder form (sub-micron range). Since we are interested in finding a way to make a lithium battery integrated onto a silicon chip we need to find a solution to this materials problem. It is envisaged that the principal applications area for lithium batteries integrated into a chip would be in the medical field. Thus the well-developed practice of cochlea implants appears to be an area that would benefit from an integrated battery supply[5].

This invention seeks to realise the potential of the

silicon-lithium system to allow the possibility of a lithium battery integrated on to a silicon chip.

Accordingly this invention provides a method of fabricating sub-micron silicon electrode structures on a silicon wafer. Preferably these structures comprise pillars.

For a silicon-lithium system the basic cell diagram can be represented as $Li|Li^+$-electrolyte$|Si$, for this cell the cathodic process is, discharge of lithium onto silicon to form an alloy (charging), and the anodic process is lithium extraction or de-alloying (discharging). The EMF data reported by Wen and Huggins[6] for the liquid system at 415°C is shown bracketed below and the solid system at room temperature[7] is shown un-bracketed below. Their results (in mV vs, Li) are: $Si/Li_{12}Si_7$-582(332); $Li_{12}Si_7/ Li_7Si_3$-520(288); $Li_7Si_3/ Li_{13}Si_4$-428(158); $Li_{13}Si_4/ Li_{21}Si_5$--~300(44).

It will be appreciated that the formation of $Li_{12}Si_7$ in place of Si results in a significant volume change (the alloy is 2.17 times bigger). On a conventional silicon wafer suitable for use as an anode for a lithium battery this volume change leads to crack formation and pulverisation however due to their small size and configuration sub-micron anode structures made in accordance with the invention, are be able to tolerate the conditions occasioned by the massive volume changes occasioned by lithium alloying/de-alloying.

In tests structured electrodes of sub micron diameter Si pillars maintained their structural integrity throughout the cycling whereas planar Si electrodes showed cracks (2 micron features) after 50 cycles. An appropriate size restriction to achieve suitable electrodes is that the silicon pillars should not exceed a fractional surface coverage (F) of ~0.5.

An embodiment of the invention will now be described by way of non-limiting example only, with reference to the accompanying drawings, in which:

Figure 1 is a schematic view of a structured electrode;

Figure 2 shows one of a series of CV scan sets;

Figure 3 shows results for a series of galvanostratic measurements;

Figure 4 shows pictures of the structure;

figure 5 shows SEM pictures of the structure; and

Figure 6 shows a lithium battery in accordance with the present invention.

The electrochemical discharge of lithium on silicon and its subsequent chemical reaction destroys the silicon lattice, giving rise to the swelling of the solid, producing amorphous Si/Li phases[13]. The first new phase to appear in

the system is $Li_{12}Si_7$. This compound, and all the rest up to Li, is a so-called Zintl-Phase Compound (ZPC), and consists of simple, electropositive, cations and complex co-valently bound, multiply charged, electronegative, anions. Of course the charge ascribed to the "ions" is purely notional: the actual charge (depending upon definition) is less than the formal value and may be considerably less, hence the bulk lithium will be referred to as Li° and bulk silicon as Si_n°.

It is important to form some idea of the mechanism of lithiation and de-lithiation of silicon. It is proposed that:

(i) Discharged lithium reacts with silicon forming a ZPC film with atomically continuous contact to the silicon.

(ii) Lithium excess diffuses (via a vacancy mechanism) through the compact ZPC film to react with silicon at the Si/ZPC interface, thickening the ZPC film, without void formation.

These processes might be represented by: $Li^+(el) + e^-(solid) \rightarrow Li(ads.)$; $Li(ads.) + V(ZPC) \rightarrow Li^\circ (ZPC)_s$; $Li^\circ (ZPC)_s \rightarrow$diffusion $\rightarrow Li^\circ (ZPC)_{ZPC/Si}$; $x\ Li^\circ + y Si^\circ \rightarrow ZPC\ (Li_{x/y}Si)$.

(Li(ads) is Li adsorbed on ZPC; V is a Li° vacancy in ZPC)

(iii) The amorphous[13] ZPC film is deformable and so does not give rise to significant stress induced cracking on volume change.

The diffusion coefficient, D, for Li in crystalline Si[14] is $\sim 10^{-14} cm^2 s^{-1}$, Li in ZPC is expected to be faster; a value of D

$10^{-12}cm^2s^{-1}$ would be enough to account for all the processes carried out in this study. This model for ZPC film formation is in many ways analogous to the model of SiO_2 layer formation on silicon due to Deal and Grove[15]: but the details are different and will be treated elsewhere.

The model for ZPC decomposition is, in broad terms, the reverse of the above steps. Discharge of Li° at the electrolyte interface produces a surface vacancy in the ZPC. Locally Li° moves into the vacancy so the vacancy diffuses back to the ZPC/Si interface: at the interface Si_n rejoins the Si phase (where it is said to be polycrystalline[13]) and vacancies coalesce to produce larger void spaces. These spaces, as they coalesce further and grow, give rise to the crack like features seen in the SEM pictures in Figures 4c,d and 5. Such a process has been described by Beaulieu et al[16] for lithium removal from silicon/tin alloys.

It has been shown that repeated Li alloying/de-alloying of planar Si can be carried out without pulverisation of the substrate, cf. Fig. 5. However, as noted, the alloy/de-alloy process is limited by diffusion through the ZPC layer. In order to obtain charging rates suitable for various applications it is necessary to increase the surface area of the Si/electrolyte interface; and this has been done using pillar fabrication. Previous attempts using silicon particles have failed because the particle-to-particle contacts change and part with cycling[2]. The pillar structures, on the other hand, are largely maintained as evidenced by the flatness of the pillar tops after 50 cycles, cf. Fig. 4.

Efficiencies of <100% reported here are attributed mainly to reaction, on alloying, with the electrolyte, and to a lesser extent isolation of regions of ZPC. The data presented here show that reduced current density on both alloying and de-alloying results in improving efficiency. It is supposed that this improvement comes mainly from a reduced surface concentration of adsorbed Li on alloying and accessing all the lithium in the ZPC on de-alloying.

There is large scope for further increasing the surface-to-volume ratio of the pillar construction, for example, pillars of diameter (d) ~0.3 microns and 6 micron height (H). The pillar volume (v) would be, FH, and for F=0.4, $v=2.4\times10^{-4}$ cc/cm^2, which is equivalent, when converted to $Li_{12}Si_7$, to a capacity of $3.81\times10^3 v$ = 914microAhrcm^{-2}. The surface area of such a pillar structure is ~4FH/d, which is the basis of the much improved characteristics.

To make structures in accordance with the invention the following method may be used, namely "Island Lithography" as disclosed in international patent No. WO01/13414. This method employs cesium chloride as the resist in the lithographic step in the fabrication of pillar arrays. It works as follows. A thin film of CsCl is vacuum deposited on the clean, hydrophilic, surface of the Si substrate. This system is then exposed to the atmosphere at a controlled relative humidity. A multilayer of water adsorbes on the surface, the CsCl is soluble in the water layer (being more soluble at places of higher radius of curvature). The CsCl re-organises into a distribution of

hemispherical islands, driven by the excess surface energy associated with CsCl surface curvature. Such arrays are useful in making structures for various studies involving nano-scale phenomena. In this case reactive ion etching is preferably used, with the islands acting as X masks so that removal of the surrounding silicon forms the desired pillar structures.

A study of the kinetics of the formation of island arrays has been carried out on GaAs surfaces[9] and more recently, and more extensively, on Si/SiO_2 surfaces[10] where the technique and results are described in detail. The process variables are: CsCl film thickness (L); humidity (RH), time of exposure (t). The resulting island array has a Gaussian distribution of diameters, average diameter (<d>) standard deviation (±s) and surface fractional coverage (F). Having made the CsCl resist array the next step is reactive ion etching (RIE) to produce the corresponding array of pillars[11]. The RIE process variables are: feed-gas composition, flow rate and chamber pressure; RF power; dc bias; etch time. The results are characterised by the etch depth, corresponding to pillar height (H), and the wall angle, namely the angle that the pillar wall makes with the wafer plane; it is chosen in this study to be close to 90°. The examples reported in this work were etched in a Oxford Plasmalab 80 apparatus. The etch gas was (O_2:Ar: CHF_3) in the ratio 1:10:20; feed rate 20sccm; chamber pressure, 50 milli pascals; RF power, 73 watts; dc bias 200V.

The pillar structure reported in this study (K-series) was characterised as <d>=580nm±15nm; F=0.34; H=810nm: it was made using, L=80nm; RH=40%; t=17.5hrs. After

fabrication the silicon samples were washed in water; etched for 20 seconds in NH_4OH(28w% NH_3):H_2O_2(100v/v):H_2O in equal volume ratios; the etchant was flooded away with de-ionized water and blow dried.

Of course the structures may also be fabricated by other known techniques, such as photolithography, which produce regular arrays of features rather than the scattered distribution produced by island lithography.

Figure 1 is a schematic view of a structured electrode, in accordance with the invention and as used in the following tests, it shows a part sectional view of the anode in which the pillars 2 can clearly be seen on the silicon wafer 3.

Figure 6 shows a lithium battery, comprising a typical embodiment of the present invention, and including an anode 1, a cathode 4, a polymer electrolyte 5, a first strip 6 representing a rectifier circuit connected to a coil encircling the anode for charging purposes, a second strip 7 representing the output circuit (driven by the battery), and a pair of wires 8 for connection to the device to be driven.

Electrochemical tests were performed in a three-electrode, glass, cell where the Si sample is the working electrode and metallic Li is used for both the counter and reference electrodes. A 1 M solution of $LiClO_4$ (Merck Selectipurâ) in ethylene carbonate:diethyl carbonate (Merck Selectipurâ), (1:1) w/w solvent was used as the electrolyte. The cell was assembled under a dry argon atmosphere in a glove box. Ohmic contact was made to the rear side of the silicon samples electrodes using a 1:1 In-Ga eutectic

alloy[12]. The electrode area was delineated using an O-ring configuration in a PTFE holder. No adhesive is used and a good electrolyte/atmosphere seal is obtained. In an earlier study we found that epoxy adhesive, used to mount a Si electrode, contaminated the active electrode surface causing spurious currents at high voltages (>2V).

Electrochemical behaviour of the cell was investigated by cyclic voltammetry (CV) and by galvanostatic measurement (voltage vs. time at constant current), using an electrochemical workstation (VMP PerkinElmer™ Instruments). The capacity referred to here is the total charge inserted into the projected electrode surface area exposed to the electrolyte (this ignores any surface area due to structuring), given as $mAhcm^{-2}$ (micro Amp hours cm^{-2}).

The results obtained were:

The response of the Li|Li^+-electrolyte|Si cell was measured: for this cell the cathodic process is, discharge of lithium onto silicon to form an alloy (charging), and the anodic process is lithium extraction or de-alloying (discharging). Figure 2 shows one series of CV scan sets (details in caption). The first cycle, and to quite a large extent the second, differs from those that follow. It is conjectured that this difference is due to a "formation" effect, associated with the filming of the electrode during the first Li discharge. After the first and second cycles, the scans assume a repeatable general shape. Since these are scans in which the potential is changed slowly and the current densities are therefore small, there are no IR drop or diffusion overpotential terms, and assuming no activation

overpotential, the electrode potential is a measure of the surface lithium activity. The first cathodic feature is the rapid increase in current at ~330 mV that, according to room temperature data[7], corresponds to the presence of $Li_{12}Si_7$. The lowest potential reached is 25mV and this is taken to be associated with the presence of higher Li compounds, e.g. $Li_{21}Si_5$. The cycling sequence shows a progressive "activation" of the sample, associated with increasing breakdown of the crystalline silicon structure (see discussion). The anodic, part of the CV curve is associated with progressive de-lithiation of the electrode according to the various ZPC equilibrium potentials. For a scan rate of 1 mVs^{-1} the capacity (260$mAhcm^{-2}$) of the electrodes is roughly comparable to the pillar volume being converted to $Li_{12}Si_7$, while for the slower scan rates the capacity exceeds that of the pillar volume. The latter results point to the participation of the substrate in the alloying/de-alloying process.

Figure 3 shows the results for a series of galvanostratic measurements on structured Si at two different charge/discharge current densities (details in caption).

Figure 4 shows the structure of the K-series of silicon electrodes that were used in this study and the effects of extensive galvanostatic cycling upon that structure. The structure are clearly intact, but at the higher current density slight cracking of the bulk Si surface, below the pillars, is observed.

Figure 5 shows the SEM pictures of the structures obtained on planar (un-pillared) Si electrodes before cycling and, separately, after galvanostatic cycling. When cycled at the lower current densities, the surface is deformed, though crack formation does not occur. Cycling at higher current densities produces wide cracks.

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Claims:

1. An integrated silicon electrode for a battery, comprising a regular or irregular array of sub-micron silicon structures fabricated on a silicon substrate.

2. A silicon anode comprising an electrode according to claim 1, in which the sub-micron silicon structures comprise pillars of silicon fabricated on an n-type silicon substrate.

3. A silicon anode according to claim 2 made on a wafer-bonded silicon-on-insulator substrate.

4. A silicon anode according to claim 2 or claim 3 in which the silicon pillars do not exceed a fractional coverage of 0.5 of the substrate.

5. A silicon electrode according to any one of the preceding claims formed by the steps of:

(a) depositing a very thin film of a highly soluble solid onto a flat hydrophilic silicon substrate;

(b) exposing the film to solvent vapour under controlled conditions so that the film reorganises into an array of discrete hemispherical islands on the surface; and

(c) reactively ion etching the silicon substrate with the islands of highly soluble solid acting as a resist so that the exposed silicon is etched away leaving pillars corresponding to the islands.

6. A silicon anode according to any one of the preceding claims wherein the pillars are 0.1-1.0 microns in diameter (d) and 1-10 micron in height (H).

7. A silicon anode according to any one of the preceding claims wherein the pillars are ~0.3 microns in diameter (d) and 6 microns in height (H).

8. A lithium battery including an anode in accordance with any one of the preceding claims.

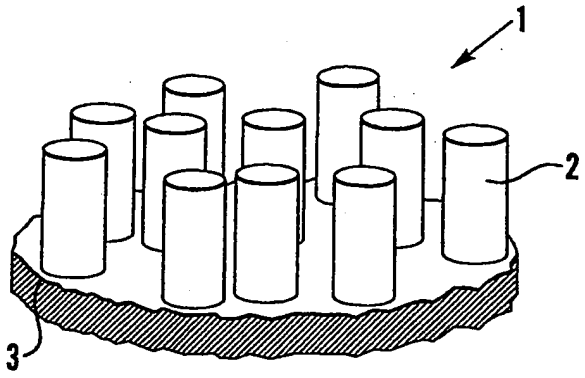


Fig. 1

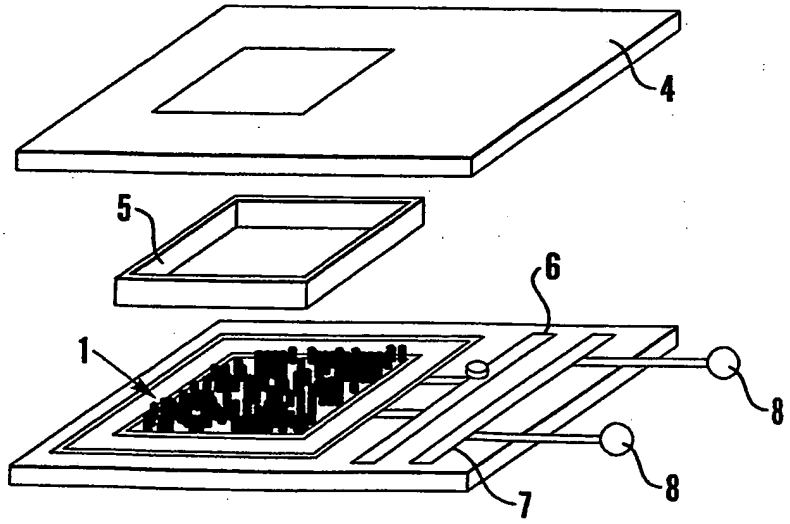
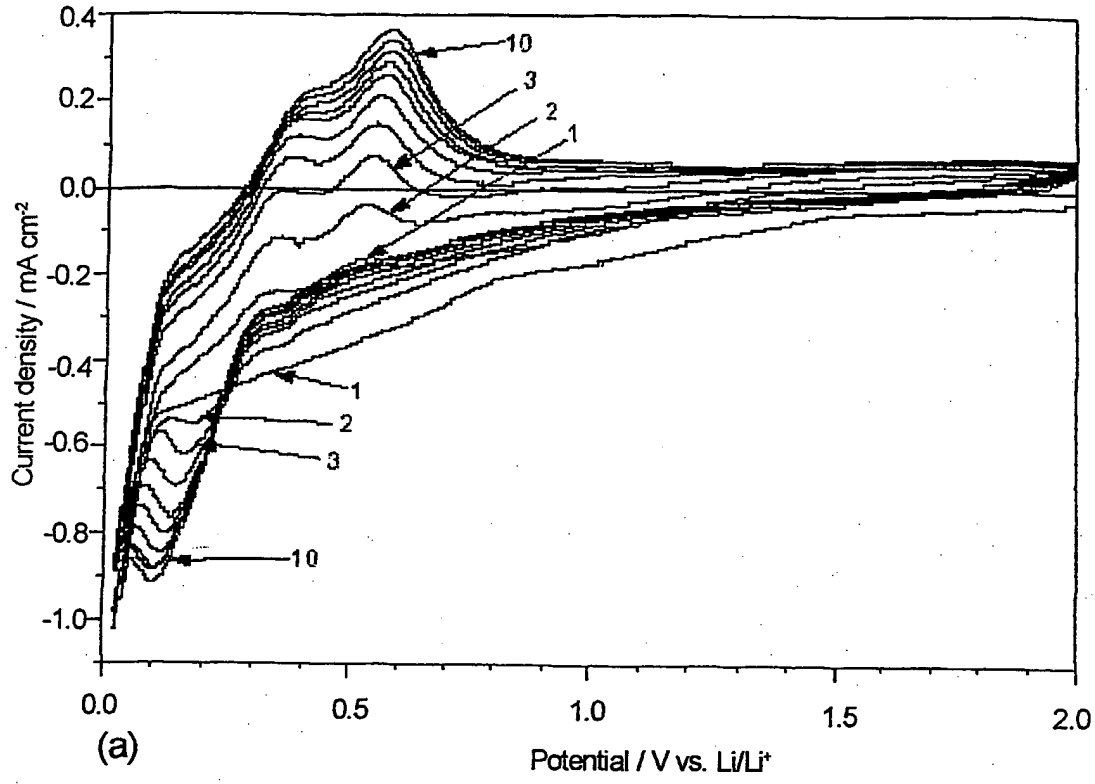


Fig. 6


0.4
0.2
0.0
-0.2
-0.4
-0.6
-0.8
-1.0
Current density / mA cm-2
10
3
2
1
1
2
3
10
0.0
0.5
1.0
1.5
2.0
Potential / V vs. Li/Li+
(a)

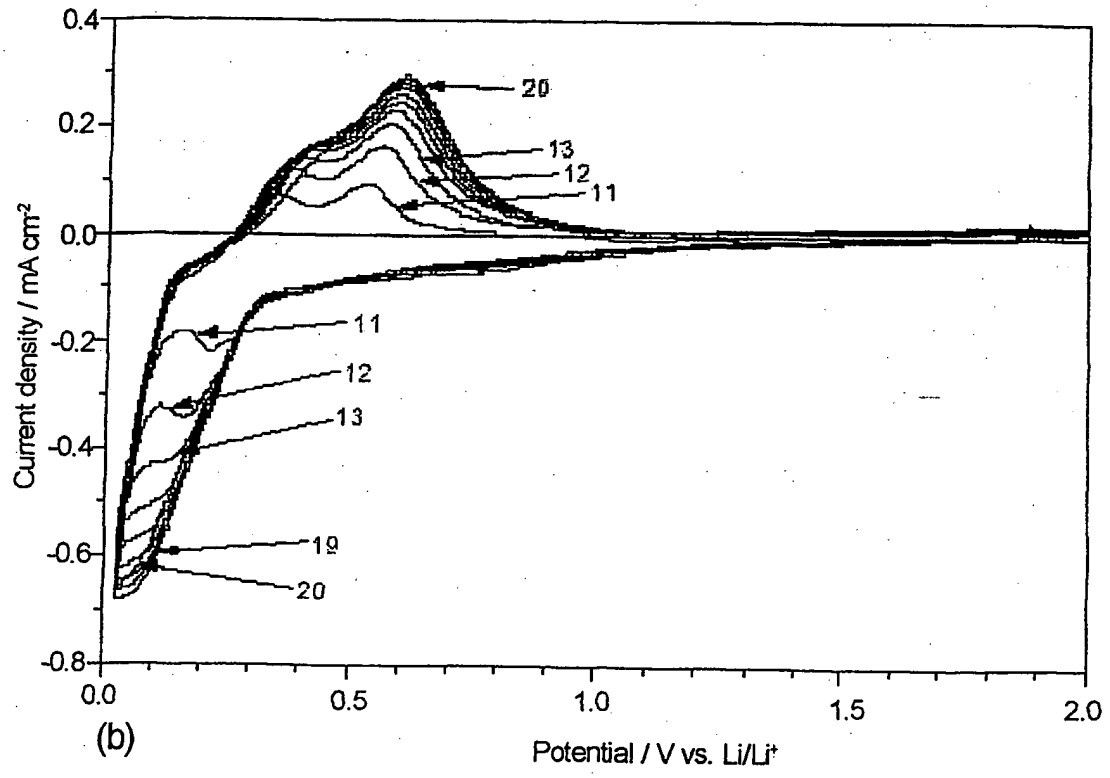
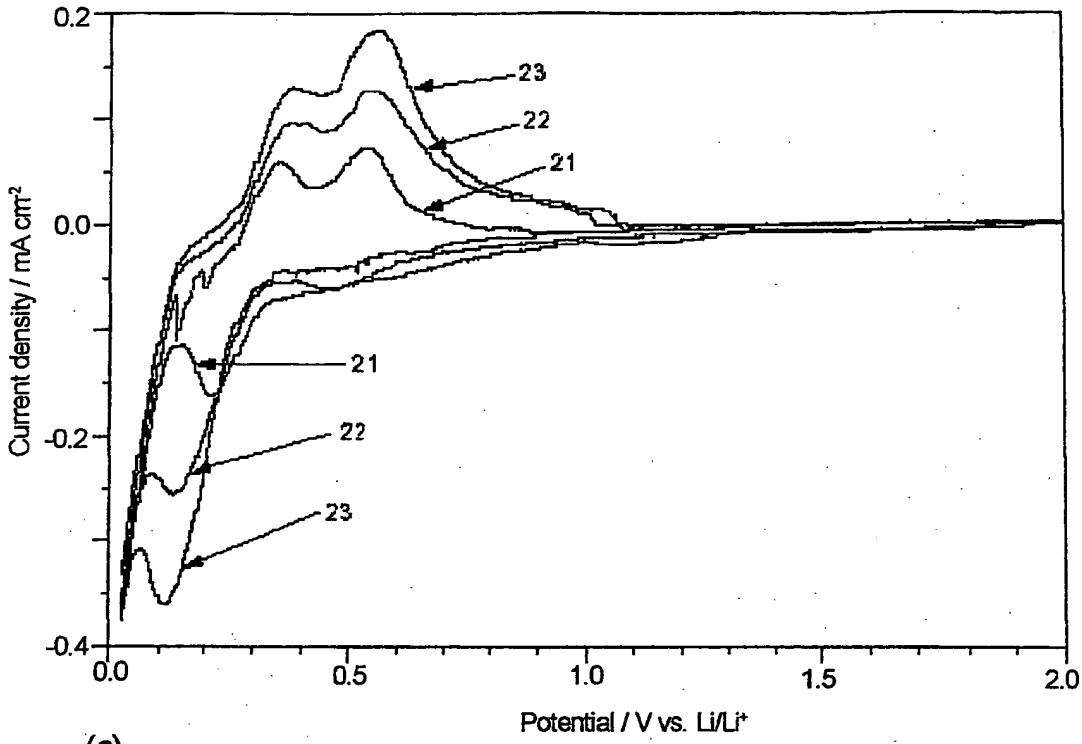
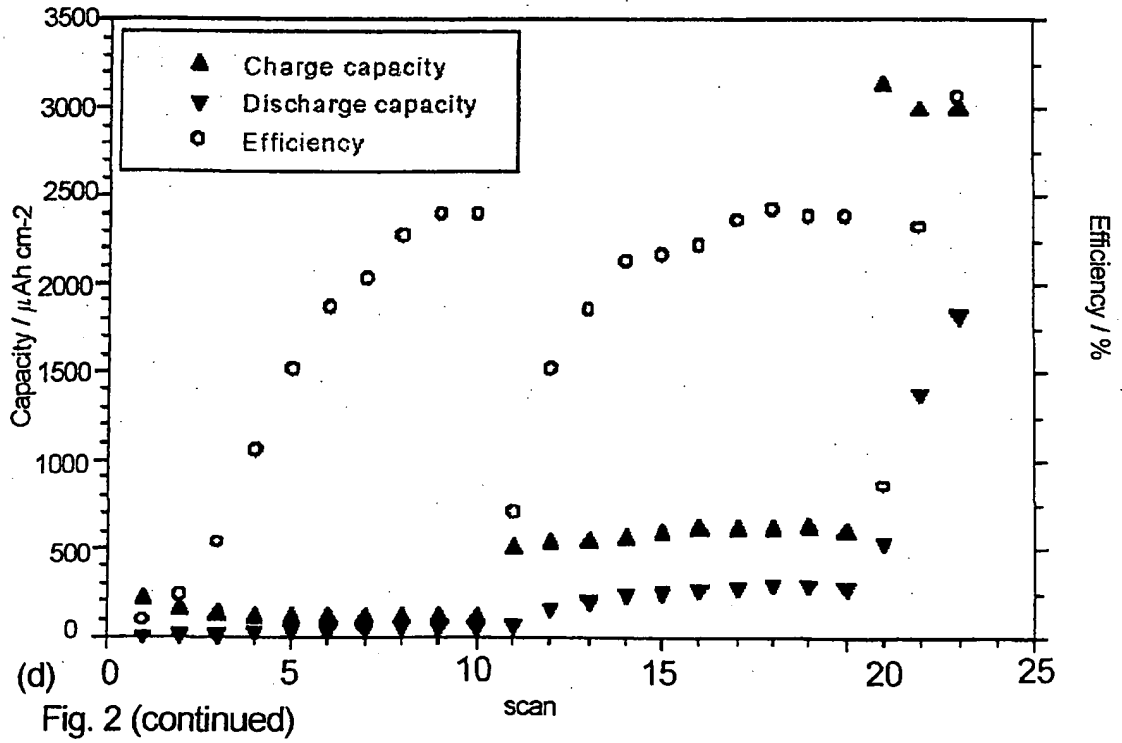

0.4
0.2
0.0
-0.2
-0.4
-0.6
-0.8
Current density / mA cm-2
20
13
12
11
11
12
13
19
20
0.0
0.5
1.0
1.5
2.0
Potential / V vs. Li/Li+
(b)

Fig. 2

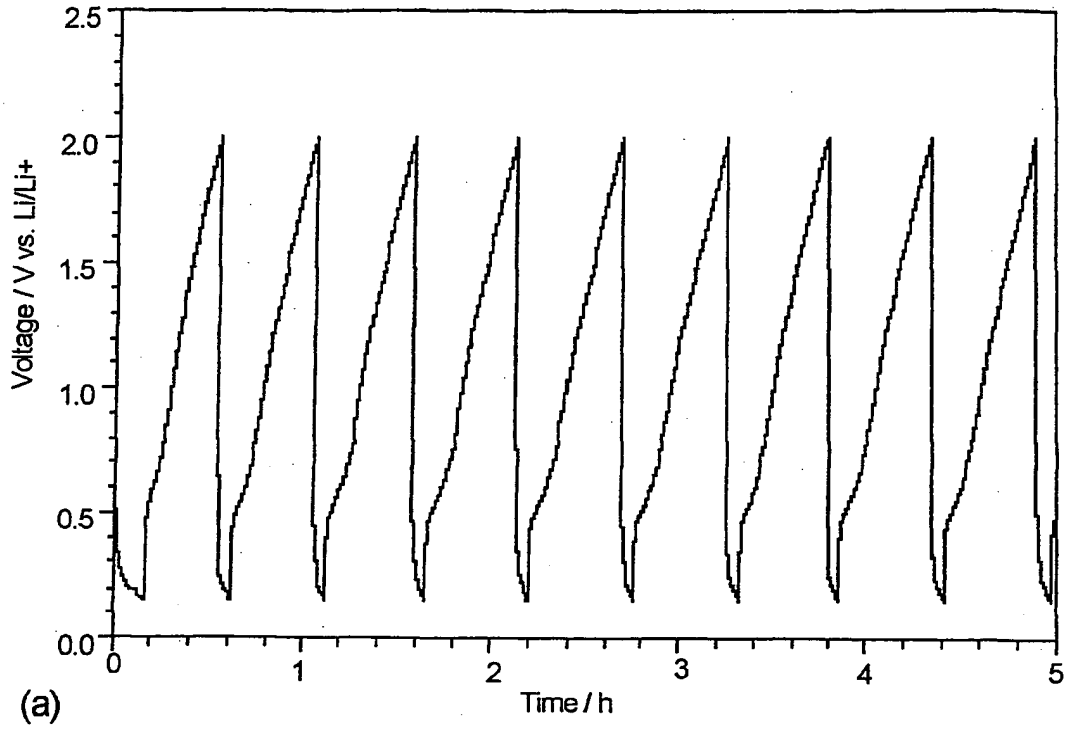


(c)



(d)

Fig. 2 (continued)


Voltage / V vs. Li/Li+
Time / h
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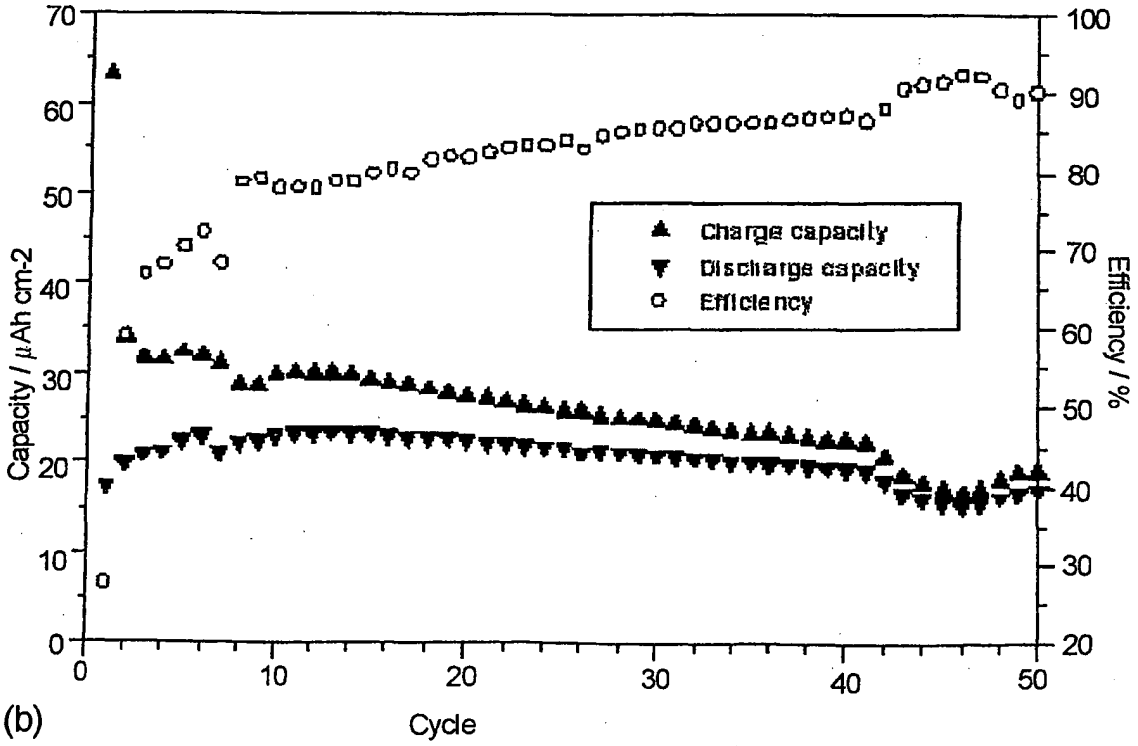
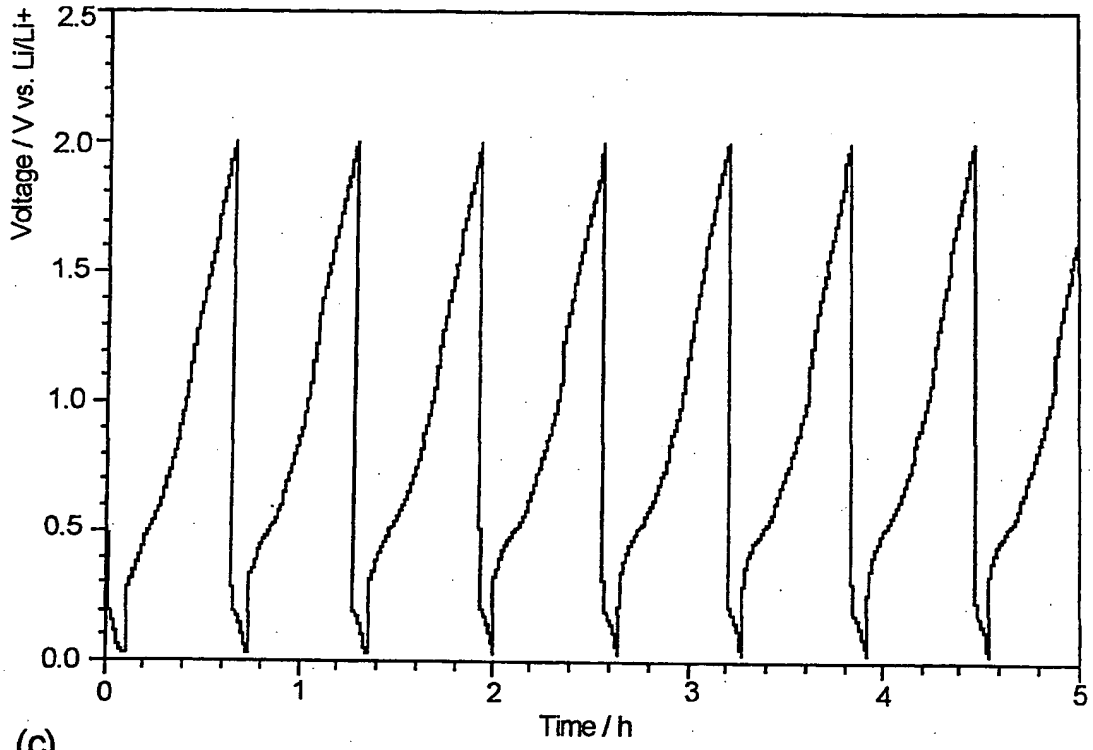
2.0
1.5
1.0
0.5
0.0
0
1
2
3
4
5

(a)

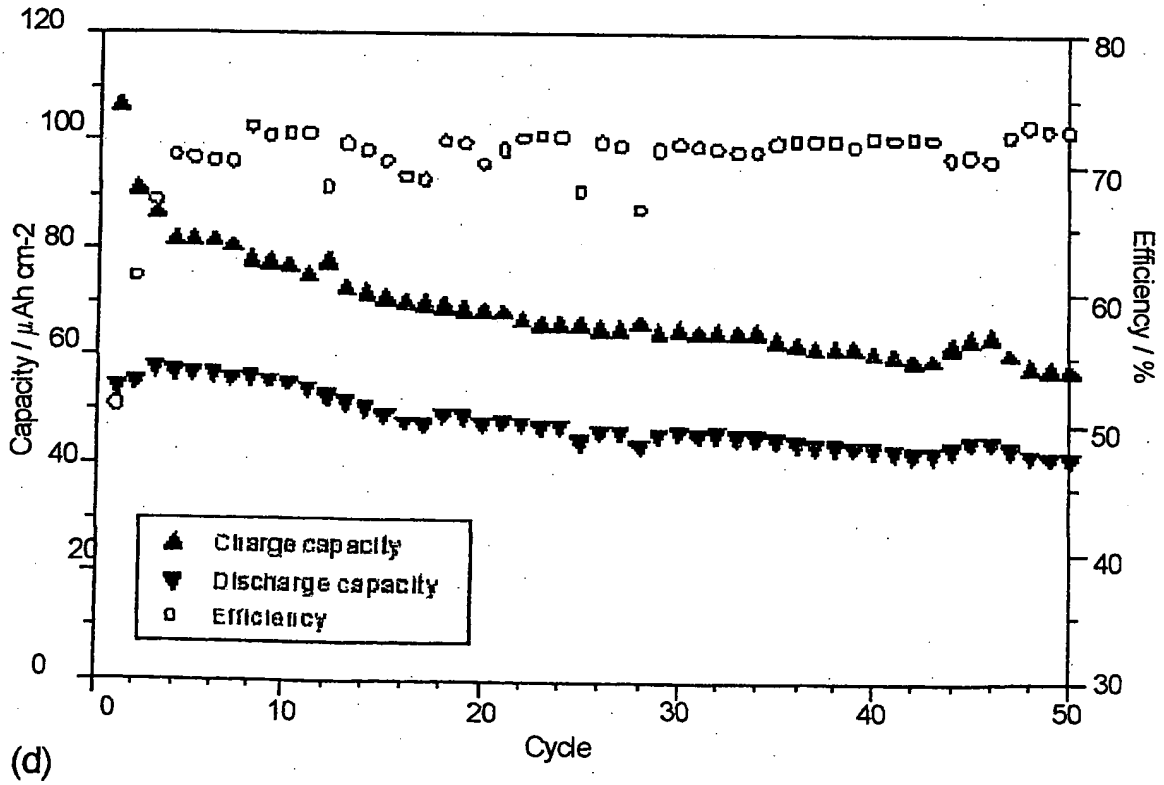

Capacity / μAh cm-2
Efficiency / %
Cycle
Charge capacity
Discharge capacity
Efficiency
70
60
50
40
30
20
10
0
100
90
80
70
60
50
40
30
20
0
10
20
30
40
50

(b)

Fig. 3

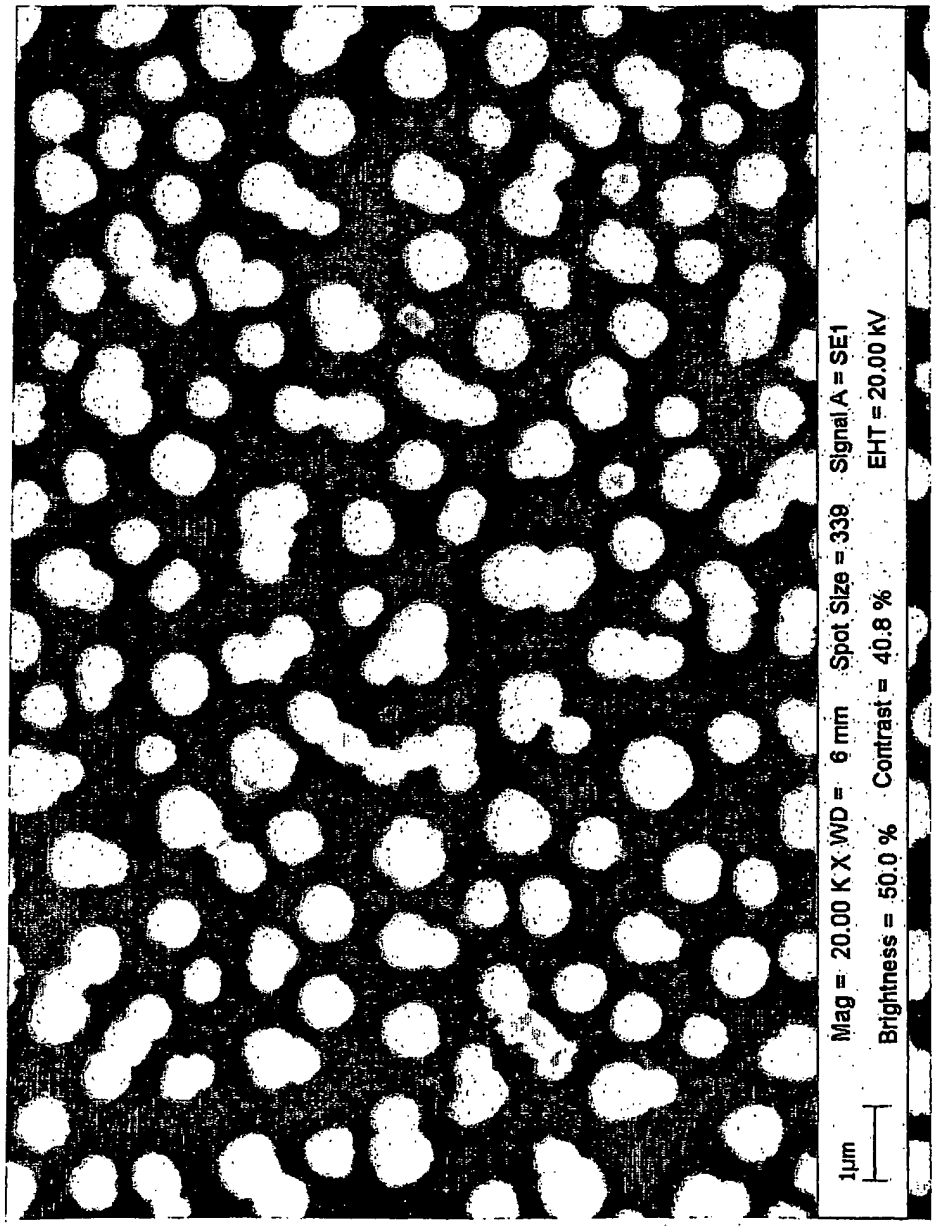


(c)



(d)

Fig. 3 (continued)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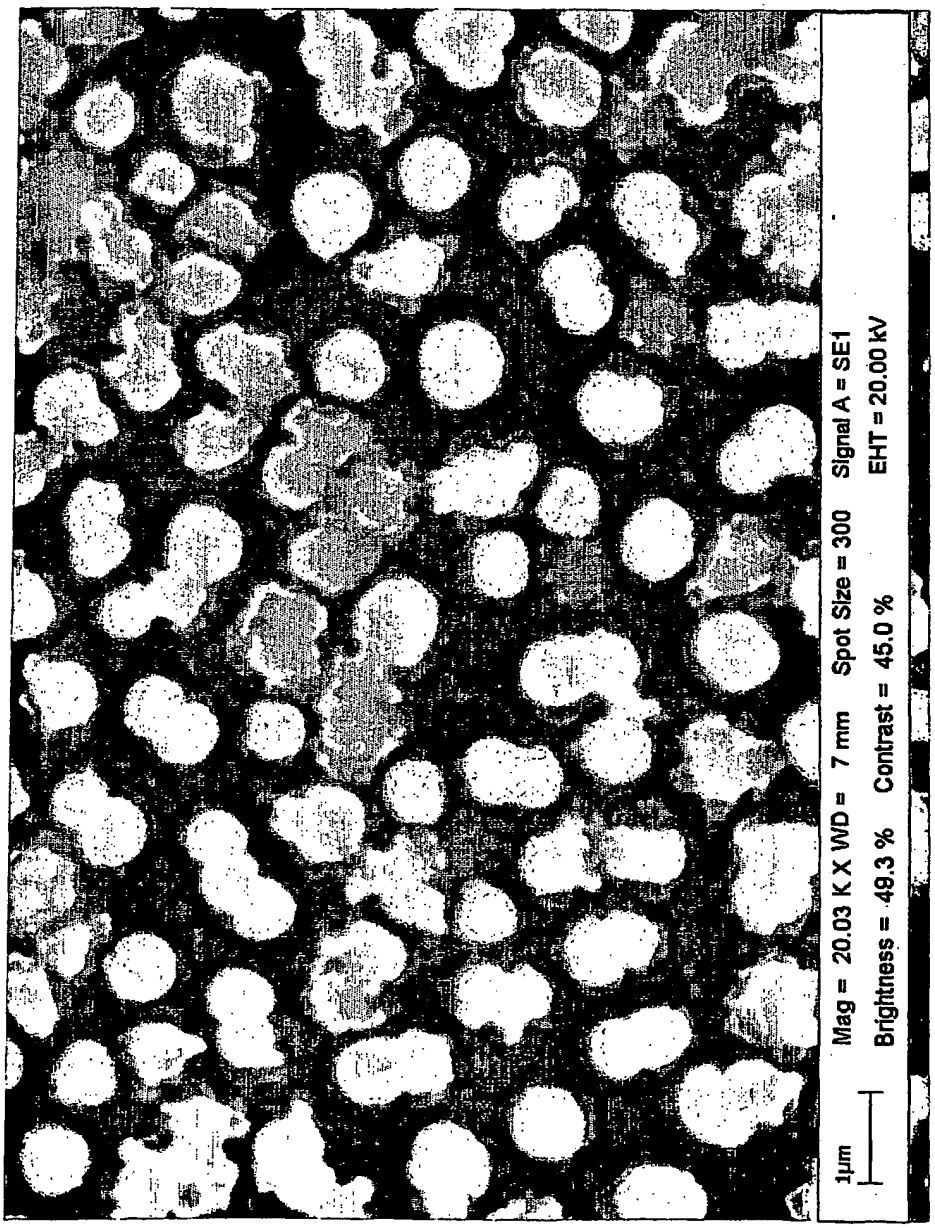
Brightness = 50.0 % Contrast = 40.8 % EHT = 20.00 kV

Fig 4 (a)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Mag = 20.03 K X WD = 7 mm Spot Size = 300 Signal A = SE1
Brightness = 48.3 % Contrast = 45.0 % EHT = 20.00 kV

Fig 4 (b)

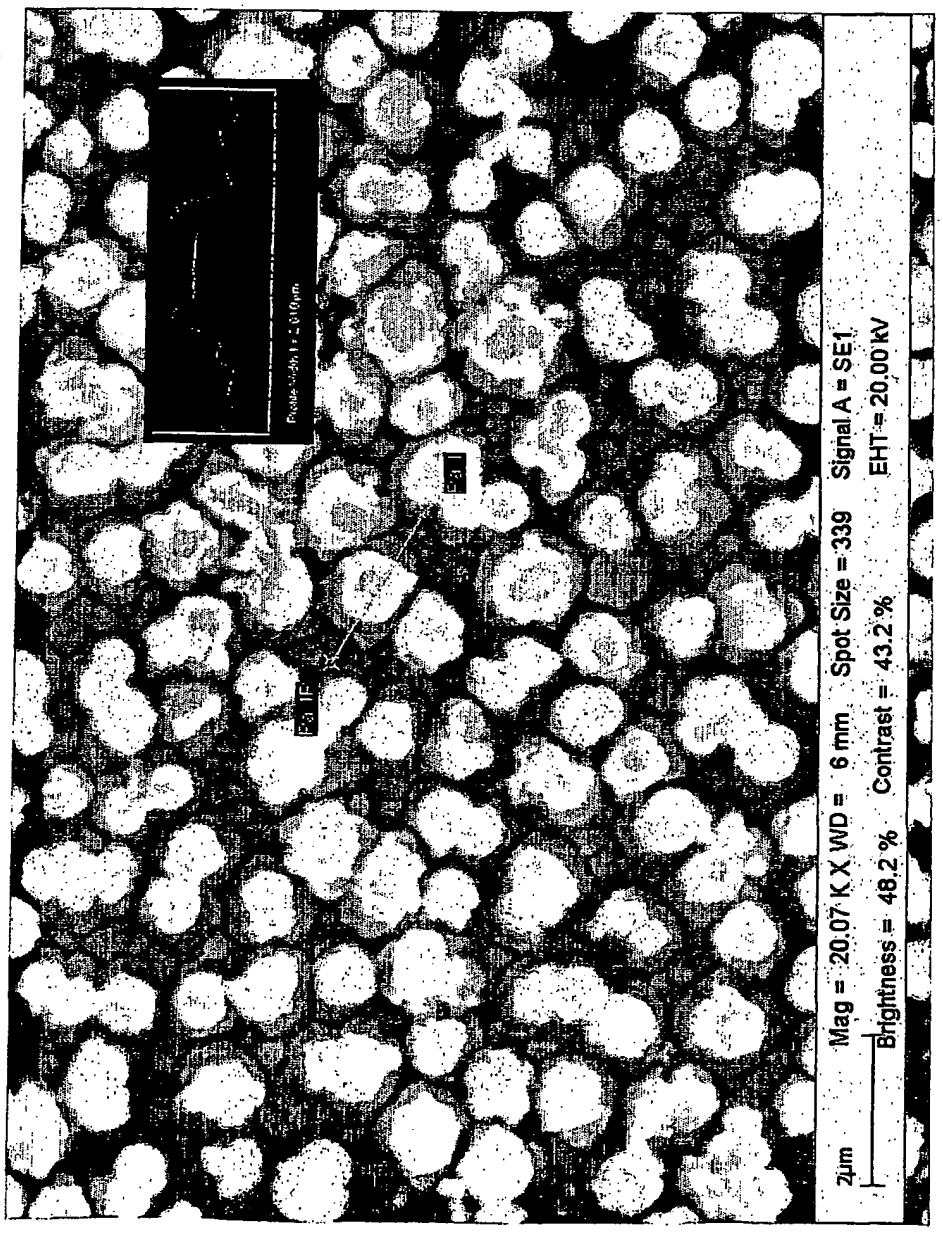
2µm
Mag = 20.07 K X WD = 6 mm
Spot Size = 339
Signal A = SE1
Brightness = 48.2 %
Contrast = 43.2 %
EHT = 20.00 kV

Fig 4 (c)

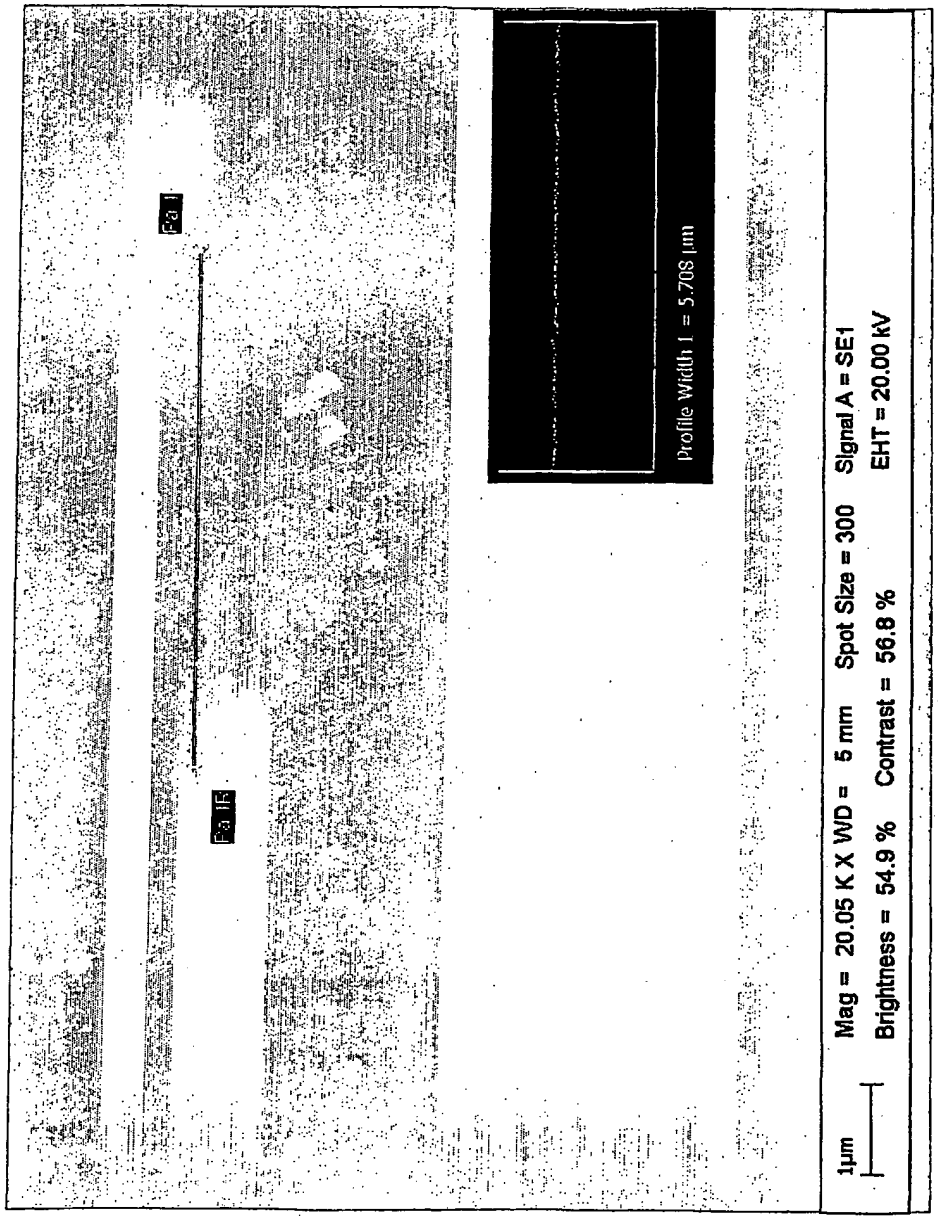
Fe I
Fe II
Profile Width 1 = 5.708 µm
1µm
Mag = 20.05 K X WD = 5 mm Spot Size = 300 Signal A = SE1
Brightness = 54.9 % Contrast = 56.8 % EHT = 20.00 kV

Fig 5 (a)

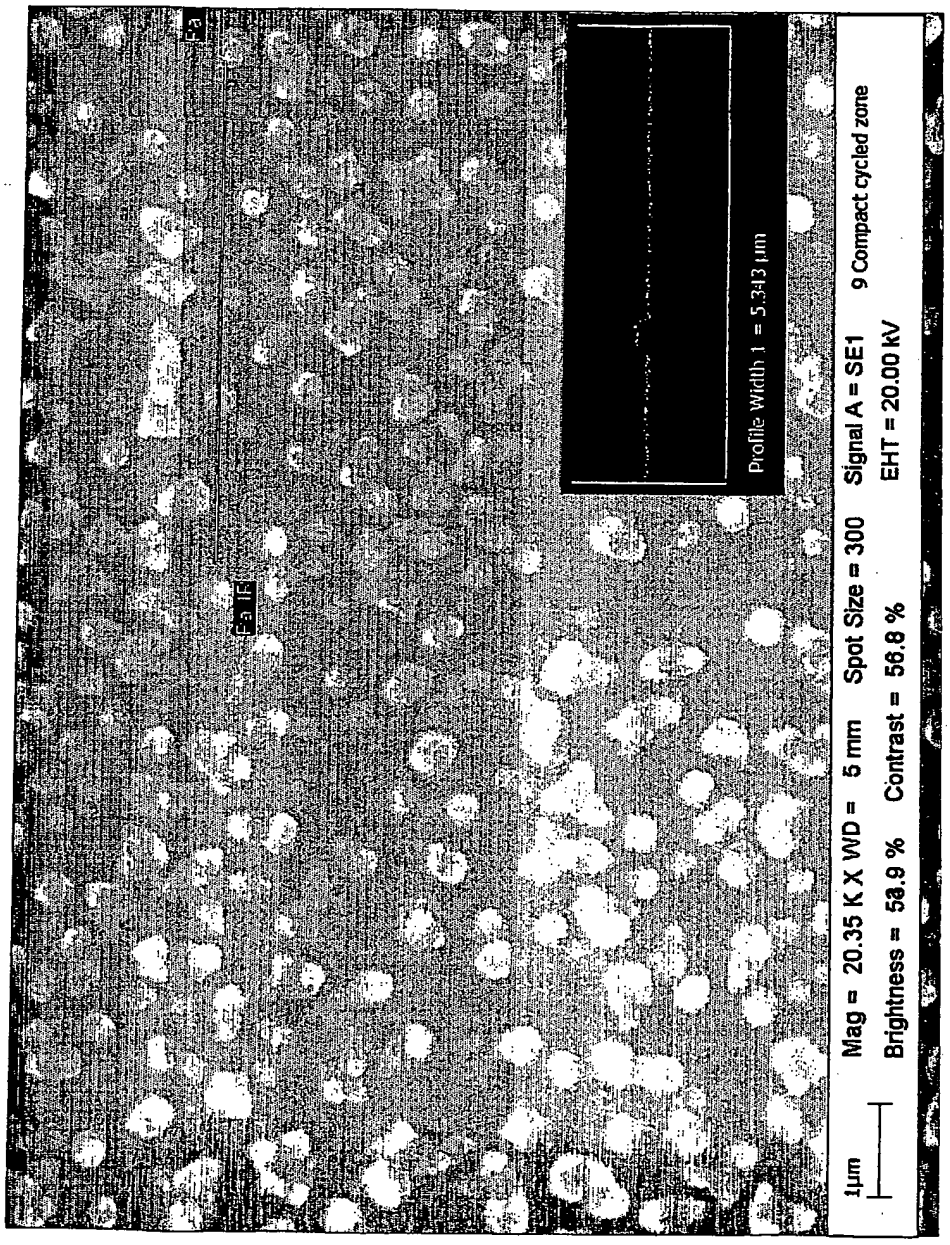
Profile Width 1 = 5.343 µm
1µm
Mag = 20.35 K X WD = 5 mm Spot Size = 300 Signal A = SE1 9 Compact cycled zone
Brightness = 58.9 % Contrast = 56.8 % EHT = 20.00 kV

Fig 5 (b)

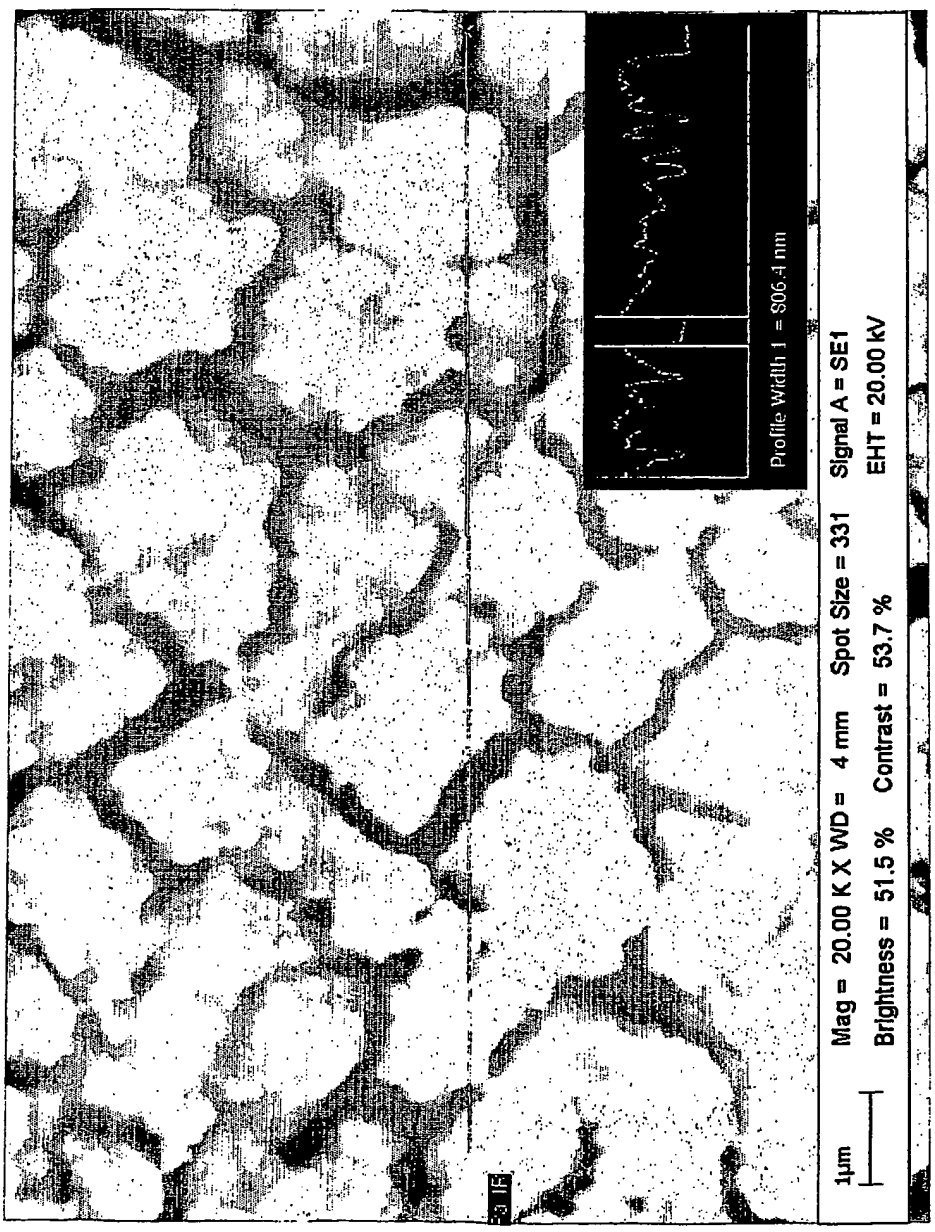
Profile Width 1 = 906.4 nm
1µm
Mag = 20.00 K X WD = 4 mm Spot Size = 331 Signal A = SE1
Brightness = 51.5 % Contrast = 53.7 % EHT = 20.00 kV

Fig 5 (c)

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